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EXAMINER	
MOLL, JESSE R	
ART UNIT	**PAPER NUMBER**
2181	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/29/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/039,579	RODGERS ET AL.	
	Examiner	Art Unit	
	Jesse R. Moll	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 October 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *70-76,79-92,98-115 and 117-121* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *70-76,79-92 and 117-121* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 December 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *23 October 2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Withdrawn Objections / Rejections

1. Applicant, via amendment, has overcome the objection to the drawings. The objection has been respectfully withdrawn.

2. Applicant, via amendment, has overcome the objection to claim 78, the objection is respectfully withdrawn.

3. Applicant, via amendment, has overcome the rejection of claims 89-92 under 35 U.S.C. 112 second paragraph. The rejection has been respectfully withdrawn.

Claim Objections

4. Claim 117 is objected to because it should end in a period.

5. Claim 120 is objected to because "being suspended; partitioning a" should read "being suspended; and partitioning a". Appropriate correction is required.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7. Claims 70-76, and 79-92 are rejected under 35 U.S.C. 102(e) as being anticipated by Emer et al. (U.S. Patent No. 6,493,741) herein referred to as Emer et al.'741.

Referring to claim 70, Emer et al.'741 discloses as claimed, a processor (CPU 100 see Fig. 2) comprising: a plurality of execution units (thread processing units TPU #1 to TPU #N see Fig. 2) to execute a plurality of threads; suspend logic (certainly inside the Emer et al.'741's system, such as a control unit, see Fig. 2) to set a monitor address (lock address 139 in memory 137, see Fig. 2) in response to a first instruction (such as LDQ ARM R1, (R5), see Col. 6, line 56) in a first thread according to an implicit operand in a predetermined register (event identification register 103, see Figs. 2 and 7) and to suspend the first thread in response to a second instruction (such as QUIESCE instruction, see Col. 6, lines 55-59) of the first thread; a monitor (event monitor 109, see Fig. 2) to cause resumption (see Col. 6, lines 1-6 regarding the TPU resumes

execution) of the first thread in response to a memory access (see Col. 6, lines 1-6, regarding a change to the lock 139 referenced in the event identification register 103) to the monitor address.

As to claim 71, Emer et al.'741 also discloses: the processor of claim 70 wherein said monitor is to cause resumption of the first thread in response to events that cause a translation look-aside buffer to be flushed (since Emer et al.'741's system certainly uses a virtual addresses using "virtual" registers, and mapper 361, see Fig. 4, is best reasonably and broadly interpreted as a translation look-aside buffer see Col. 6, lines 40-49).

As to claim 72, Emer.et al.'741 also discloses: the processor of claim 70 wherein said monitor is to cause resumption of the first thread in response to a write to a control register CRO (see Col. 5, lines 39-40, regarding the write to a specified location in memory space and this the situation the location is a control register).

As to claim 73, Emer et al.'741 also discloses: the processor of claim 72 wherein said monitor is to cause resumption of the first thread in response to an interrupt (see Col. 5, lines 39-40, regarding the write to a specified location in memory space and note the write will eventually cause an interrupt for the I/O operation) being one of a non-maskable interrupt and a system management interrupt.

Note that any interrupt in a system can be considered to be a system management interrupt. An interrupt manages the system.

As to claims 74 and 75, Emer et al.'741 also discloses: as best understood, said suspend logic (as set forth this is certainly inside the Emer et al.'741's system, such as

a control unit comprising Quiesce Logic 110 see Fig. 2) is only to suspend said first thread if said monitor address (Lock 139, see fig. 2) is a selected memory type (the address type in memory 137, see Fig. 2).

As to claim 76, Emer et al.'741 also discloses: the processor of claim 74 wherein said selected memory type is a write-back type of memory (since the memory 137 will be updated eventually).

As to claim 78, Emer et al.'741 also discloses: the processor wherein a powerdown event is not a monitor break event (since the Emer et al.'741 does not indicate to use the powerdown event for controlling the system).

As to claim 79, Emer et al.'741 also discloses: the processor of claim 70 further comprising an instruction buffer (355 see Fig. 4, and col. 6, lines 35-39) which can be combined to form a single partition dedicated to one thread or can be partitioned to be used by the plurality of threads (see col. 6, lines 35-39).

As to claim 80, Emer et al.'741 also discloses: the processor of claim 70 further comprising a front end (comprising fetch thread chooser 301, see Fig. 3 or map thread chooser 351, see Fig. 4), which performs microoperation (uOP) generation, generating uOPs from macroinstructions (since the fetched instructions will be decoded before execution in the Emer et al.'741's system).

As to claim 81, Emer et al.'741 also discloses: the processor of claim 80 wherein said processor is capable of out-of-order execution and wherein said first instruction is followed by a store fence (this is the step when using cache-coherence protocol as indicated in col. 7, lines 51-64).

As to claim 82, Emer et al.'741 also discloses: The processor of claim 70 wherein a second operand (in the instruction such as LDQ_ARM R1, (R5), see Col. 6, line 56) specifies events to mask.

As to claim 83, Emer et al.'741 also discloses: the processor of claim 82 wherein one mask bit (such as the bit in Watch_flag 105) indicates that masked interrupts break restart the first thread (see Col. 6, lines 1-6, regarding a change to the lock 139 referenced in the event identification register 103) despite interrupts being masked.

As to claim 84, Emer et al.'741 also discloses: The processor of claim 70 wherein said first instruction is an instruction having only implicit operands (in the instruction such as LDQ_ARM R1, (R5), see Col. 6, line 56).

As to claim 85, Emer et al.'741 also discloses: the processor of claim 70 further comprising: coherency logic (since the Emer et al.'741's system use cache-coherence protocol as indicated in col. 7, lines 51-64) to perform a read line transaction in conjunction with suspending the first thread.

As to claim 86, Emer et al.'741 also discloses: The processor of claim 85 wherein said coherency logic is to perform a cache line flush to flush internal caches in conjunction (since the invalid cache data will be updated in the cache therein) with suspending the first thread.

As to claim 87, Emer et al.'741 also discloses: The processor of claim 70 wherein said processor is to monitor for a request for ownership or an invalidate cycle to the monitor address (since the Emer et al.'741's system use cache-coherence protocol as indicated in col. 7, lines 51-64).

As to claim 88, Emer et al.'741 also discloses: The processor of claim 70 wherein said processor is to assert a hit signal during a snoop phase of a bus transaction implicating the monitor address (as set forth above since the Emer et al.'741's system use cache-coherence protocol as indicated in col. 7, lines 51-64).

As to claim 89, Emer et al.'741 also discloses: The processor of claim 88 wherein the monitor is to cause said plurality of partitionable resources (such as the thread processing units TPU #1 to TPU #N see Fig. 2) to be re-partitioned to accommodate execution of said first thread in response to the memory access to the monitor address.

As to claim 90, Emer et al.'741 also discloses: The processor of claim 89 wherein said plurality of partitionable resources (the thread processing units TPU #1 to TPU #N see Figs. 2 and 6) comprise: an instruction queue (such as 305 see Fig. 2); a re-order buffer (such as 361 see Fig. 2); a pool of registers (such as 309 see Fig. 2); a plurality of store buffers (such as 403A see Fig. 6).

As to claim 91, Emer et al.'741 also discloses: The processor of claim 90 further comprising: a plurality of duplicated resources (the thread processing units TPU #1 to TPU #N see Figs. 2 and 6), said plurality of duplicated resources being duplicated for each of said plurality of threads, said plurality of duplicated resources (the thread processing units TPU #1 to TPU #N see Figs. 2 and 6) comprising:
a plurality of processor state variables; an instruction pointer; register renaming logic (the above elements are certainly existing in the SMT system such as Emer et al.'741's processor shown in Figs. 2 and 6).

As to claim 92, Emer et al.'741 also discloses: The processor of claim 91 further comprising: a plurality of shared resources (the thread processing units TPU #1 to TPU #N see Figs. 2 and 6), said plurality of shared resources being available for use by any of said plurality of threads, said plurality of shared resources comprising: said plurality of execution units (such as ALUs inside the thread processing units TPU #1 to TPU #N see Figs. 2 and 6); a cache (311 see Fig. 3); a scheduler (such as controllers inside the thread processing units TPU #1 to TPU #N see Figs. 2 and 6).

8. Claims 117-121 are rejected under 35 U.S.C. 102(e) as being anticipated by Yasuhara (U.S. Patent No. 6,463,482 B1).

9. Regarding claim 117, Yasuhara discloses a method comprising: receiving a first opcode (opcode for performing a DMA Transfer, see fig. 6) in a first thread of execution (code for executing a DMA transfer); executing a bus transaction (DMA transfer) by a monitoring bus agent (PCI monitoring unit 8, see fig. 5) to ensure no other bus agent (such as MPC transfers) has sufficient ownership of data associated with said first opcode (data on the bus) to allow another bus agent to modify the data without informing the monitoring bus agent (DMA transfers need not go through bridge circuit 7); monitoring for an access to an address associated with said first opcode (access to the PCI bus); signaling a hit if another bus agent reads said physical address (see step 102; fig. 6); and suspending said first thread of execution (see step 103; fig. 6) in response to a second opcode (opcode for performing a MPC transfer; see fig. 6).

10. Regarding claim 118, Yasuhara discloses the method of claim 117 further comprising: resuming said first thread if the access occurs (see step 105; fig. 6

Note that the DMA transfer will resume if it is suspended.);

and resuming execution of the first thread in response to any one of a first set of events (completing the MPC transfer).

11. Regarding claim 119, Yasuhara discloses the method of claim 117 wherein said bus transaction is a read bus transaction (DMA transfers can be read or write).

12. Regarding claim 120, Yasuhara discloses the method of claim 117 further comprising: relinquishing a plurality of partitioned resources (lines of the PCI bus) in response to said first thread being suspended (when the DMA transfer is suspended, the DMA transfer relinquishes the use of the multi-line PCI bus; see fig. 6); and partitioning a plurality of resources in response to said access (The PCI bus is partitioned for use by the MPC transfer).

13. Regarding claim 121, Yasuhara discloses the method of claim 117 wherein suspending said first thread of execution in response to said second opcode comprises: testing whether a monitor event is pending (DMA is being executed); testing whether a monitor operation by said monitoring agent is active (execution of MPC is shorter than a predetermined time; see fig. 6;

Note that both of these events are being monitored, therefore executing a DMA transfer is a monitor event and a short MPC transfer is a monitor operation.);

if said monitor operation is active and no monitor event is pending, then entering a first thread suspend state (see step 103; fig. 6).

Allowable Subject Matter

14. Claims 98-115 are allowed. Please refer to the Office Action mailed 07/28/05 which sets forth the reasons for allowance.

Response to Arguments

15. Regarding the drawings and the 35 U.S.C. §112, second paragraph problems, Applicant's response has not completely overcome these objections and rejections.

16. Applicant's arguments filed 30 June 2006 have been fully considered but they are not persuasive.

17. Applicant states:

> For instance, with respect to independent claim 70, it is alleged that a "control unit" inside a system taught by Emer teaches the suspend logic as claimed. More specifically, the Office Action states "suspend logic (certainly inside the Emer et al. '741's system, such as a control unit, see Fig. 2)...to set a monitor address" is taught by Emer. Seepage 4, paragraph 5 of the Office Action. Applicants respectfully disagree.
>
> First and foremost, in contrast with these allegations, there is no description of a "control unit" within the Emer system. Applicants respectfully request the Examiner to identify the component that alleging constitutes the "suspend logic" as claimed. This "suspend logic" must also suspend the first thread in response to a second instruction of the first thread.

> Withdrawal of the § 102(e) rejection as applied to independent claim 70 is respectfully requested.

Examiner disagrees. The processor disclosed by Emer et al. '741 **must** have control logic. Certain actions occur in the processor, whatever logic performs these actions is the control unit. As Emer et al. '741 shows (col. 6, lines 55-59), QUIESCE instructions can be executed to suspend a thread. There must be logic present in the processor to execute the instruction. This logic is considered to be the suspend logic.

18. Applicant states:

> For dependent claim 71, the Office Action alleges that the mapper (361) of Emer constitutes the translation look-aside buffer as claimed. See Page 8 of the Office Action. Applicants respectfully traverse the rejection, and respectfully submit that Emer fails to provide any teaching that the monitor (event monitor 109) causes resumption of the first thread in response to events that cause by the translation look-aside buffer (mapper 361 of Emer) to be flushed. Hence, withdrawal of the § 102(e) rejection as applied to dependent claim 71 is respectfully requested.

Examiner disagrees. Firstly, claim 71 merely claims a processor and states the intended use of said monitor. Further, many events would cause both a TLB to be flushed cause resumption of the first thread. One example of an event which would cause both actions to occur is a clock signal.

19. Applicant states:

> For dependent claim 73, the Office Action alleges that the limitations set forth in this claim are taught because a write will eventually cause an interrupt for the I/O operation. See Page 9 of the Office Action. Applicants respectfully disagree that Emer provides such teachings because there is no teaching of the event monitor (109) causing resumption of the first thread in response to an interrupt (e.g., NMI or SMI). Emphasis added," See Page 9 of the Office Action. Hence, withdrawal of the § 102(e) rejection as applied to dependent claim 73 is respectfully requested.

Examiner disagrees. If a LDQ_ARM instruction (such as shown in col. 6, lines 55-59) misses in the cache, it will have to go to main memory. When the instruction is fetched from memory, execution will be interrupted and another thread will be resumed. If a second thread contains a LDQ_ARM instruction, the it is actually executed (in response to it being loaded from memory), the first thread will be resumed. Further, Emer discloses that threads are resumed after a certain amount of clock cycles (col. 8, lines 43-48). The end of the time is considered an interrupt that resumes execution.

20. Applicant states:

> For dependent claim 79, the Office Action alleges that the Emer discloses an instruction buffer which can be combined to form a single partition dedicated to one thread or can be partitioned to be used by a plurality of threads. See Page 10 of the Office Action; Column 6, lines 35-59 of Emer. Applicants respectfully disagree with the allegation because Emer is exclusively directed to a multi-threaded environment and does not account for a single threaded department. See Column 6, lines 31-49 of Emer. Hence, withdrawal of the §102(e) rejection as applied to claim 79 is respectfully requested.

Examiner disagrees. The limitations of claim 79 merely state that the buffer "**can** be adapted..." The limitation only makes the adaptability of the buffer optional. Furthermore, if it was not optional, the claim only requires that the buffer "be adapted as a single partition dedicated to one thread **or** be used by the plurality of threads". The claim only requires one or the other. As the previous Office Actions states, Emer discloses that the buffer is partitioned to be used by the plurality of threads.

21. Applicant states:

> For dependent claim 80, the Office Action alleges that the Emer discloses a front end (considered to be the fetch thread chooser 301 or map thread chooser 351 of Emer). See Page 10 of the Office Action. As claimed, the front end performs micro-operation (uOP)

> generation from macroinstructions. Applicants respectfully traverse the rejection because Emer does not disclose that the fetch thread chooser (301) or the map thread chooser (351) elements with such functionality.
>
> In fact, Applicants respectfully submit that the claimed functionality would not be performed by the fetch thread chooser (301) or the map thread chooser (351), and thus, respectfully request the Examiner to provide disclosure in Emer that supports the rejection. Otherwise, withdrawal of the § 102(e) rejection as applied to claim 80 is respectfully requested.

Examiner disagrees. Instructions are decoded prior to execution. The instructions held in memory (or cache) are considered to be macroinstructions. After decoding, the representation of the instructions are considered to be micro-operations (uOPs). Therefore, the decoding of non-quiesced instructions is considered to be uOP generation.

22. Applicant states:

> For dependent claim 82, the Office Action alleges that the Emer discloses a processor wherein the second operand (in the "LDQ ARM R1, (R5)" instruction specifies events to mask. See Page 11 of the Office Action; Column 6, lines 56 of Emer. Applicants respectfully traverse the rejection, because the "LDQ ARM R1, (R5)" instruction is adapted to compute the lock's physical address from the contents of register R5, record the physical address in the event identification register (103), and load the lock value from the physical address into register R1. See col. 6, lines 61-67 of Emer. The second operand "(R5)" does not specify the events to mask as alleged in the Office Action. Withdrawal of the § 102(e) rejection as applied to claim 82 is respectfully requested.

Examiner disagrees. The load instruction is part of a lock sequence. The lock sequence as a whole is intended to mask a portion of code so that it is not executed until a corresponding resource is available. As part of the sequence, the load instruction specifies events (instructions) to mask (selectively stop execution).

Conclusion

23. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jesse R. Moll whose telephone number is (571)272-2703. The examiner can normally be reached on M-F 10:00 am - 6:30 pm EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald A. Sparks can be reached on (571)272-4201. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Jesse R Moll
Examiner
Art Unit 2181

JM 1/21/07

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SUPERVISORY PATENT EXAMINER